An Ultra-Low-Power 15-bit Digitally Controlled Oscillator with High Resolution

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Abstract
In this paper, an ultra low power 15-bit digitally controlled oscillator is proposed. The proposed DCO is designed based on a segmental coarse-tuning stage and employs hysteresis delay cell (HDC) and digitally controlled varactor (DCV) in the fine-tuning stage. The proposed circuit has a simple structure, and the power consumption of this design is very low. Simulation of proposed DCO using TSMC 180nm model achieves controllable frequency range of 205MHz ~ 925MHz with a wide linearity. Monte Carlo simulation demonstrates that the time-period jitter due to random power supply fluctuation is under 90 ps and the power consumption is 255µW at 205MHz with 1.8V power supply.

Keywords: digitally controlled oscillator (DCO); low power; resolution; linearity; jitter

INTRODUCTION
PHASE-LOCKED LOOP (PLL) is a very important clocking circuit for many digital systems such as digital communication and microprocessor (Sheng et al., 2006). Traditional PLLs are designed by analog approaches. However, as supply voltage decreases, both gain and frequency range need to be traded off in voltage-controlled oscillator (VCO) which is the most important block in PLL. In addition, due to serious leakage current problem, it is hard to design a charge-pump circuit in more advanced process technology. Thus, it needs more design efforts to integrate analog PLLs in SoC with lower supply voltage and advanced process. Furthermore, as technology migrates, the analog blocks need to be re-designed. In contrast, all-digital phase-locked loop (ADPLL) (Sheng et al., 2006; Dunning et al., 1995; Olsson and Nilsson, 2004; Chung et al., 2003; Staszewski et al., 2007) uses the cell-based design approaches, so it can be easily integrated into the digital system (Sheng et al., 2006).

The digitally controlled oscillator (DCO) is the heart of ADPLL. Just like the Voltage-controlled oscillator (VCO) in PLL (Sheng et al., 2006). DCO dominates the major performance of ADPLL such as power consumption and jitter, and hence is the most important of such clocking circuits (Sheng et al., 2006; Dunning et al., 1995; Olsson and Nilsson, 2004; Chung et al., 2003; Staszewski et al., 2007) uses the cell-based design approaches, so it can be easily integrated into the digital system (Sheng et al., 2006).

A standard cell description of the DCO simplifies the design and can be easily ported to different process. A simple DCO that directly uses an inverter ring is presented in (Olsson and P. Nilsson, 2003), but has insufficient resolution for most applications. Another DCO example consists of bank of tri-state inverter buffers (Roth et al., 2003). The delay resolution in this case can be controlled by the number of enable buffers. However, (Roth et al., 2003) has the disadvantages of large silicon area and high power consumption. The Or-And-Inverter (OAI) cells are proposed to enhance resolution by different input pattern combinations; however linearity remains be solved (Raha et al., 2002). Although digitally controlled varactor (DCV) has a good performance in resolution and linearity (Chen et al., 2005), it is hard to take a few cells to provide wider operation range. As a result, large power consumption is demanded due to many DCV cells to maintain an acceptable operating range. The proposed DCO in this paper has largely resolved these problems.

Fig.1 shows block diagram of the proposed DCO. Our proposed DCO can save power consumption and keep resolution. To provide control code-to-delay
linearity and wide operating range the proposed DCO uses cascading structure for both coarse-tuning and fine-tuning stages. We used the following techniques to reduce the power consumption of the circuit. When the DCO operates in high frequency, the desired delay time is short. Thus the some segmental delay cells (two-input OR gates) in the coarse-tuning-stage can be disable and the power consumption can be reduces. Two-input OR gate consumes less power than two-input AND gate because of the lower switching activity, so we used the two-input OR gates in the coarse-tuning-stage delay cells. In the fine-tuning stage, hysteresis delay cell (HDC) is proposed to reduce the number of short-delay cells. Also the pass selector MUX which is used in our proposed DCO applies transmission gates instead of tri-state buffers to select the coarse-tuning-stage output path so it costs less area and lower power consumption than the conventional MUXs.

(b)

PROPOSED DIGITALLY CONTROLLED OSCILLATOR

Structure of Proposed DCO

Fig. 2 shows the structure of proposed cell-based DCO with 15 bits binary weighted control. The proposed DCO structure is separated into two stages: the coarse-tuning stage and the fine-tuning stage the higher five bits of the control code are for coarse tuning stage, and lower eight bits are for the fine-tuning stage. The coarse-tuning stage is composed of 31 two-input OR gates and the 32-to-1 path selector MUX which can provide 32 different delay values by selecting different delay path organized by these 31 two-input OR. In the conventional coarse-tuning stages reported in (Sheng et al., 2006; Chung et al., 2003; Chen et al., 2005). The coarse tuning stage delay cell is composed of buffers. When delay line is request to provide higher operation frequency, a shorter delay path is selected and the rest delay cells will not be used. However, these delay cells are not disabled. To reduce power consumption as the operating frequency changes, some enabling input controlled signals (EN [30:0]) are set low level to disable those redundant two-input OR gates, leading to save power consumption. Two input OR gate consumes less power than two-input AND gate because of the lower switching activity, so we used the two-input OR gates in the coarse-tuning-stage delay cells. The proposed 32-to-1 path selector MUX architecture is implemented with transmission gates and costs less area and lower power consumption than the conventional path selector MUXs which had used tri-state buffers in their structure. In order to reduce the loading capacitance of path selector MUX output, the path selector MUX is partitioned into two stages. in first stage, every 8 coarse-tuning delay cells will select a partial output, and the second stage path selector will select the final output. The proposed Coarse-tuning stage and path selector MUX are shown in Fig. 2 (a) and (b).

(c)
Second in order to increase resolution of DCO, a fine-tuning stage is added into the DCO design as shown in Fig. 2(c). To achieve better resolution and less power consumption, this fine-tuning stage is divided into three different substages. The delay steps of these fine-tuning substages are different; delay cells of the first stage and third stage have the largest and smallest delay step, respectively. So, delay cell of the third-tuning stage determines the DCO LSB resolution and controllable range of the first fine-tuning stage can cover delay step of the coarse-tuning stage easily. It should be noted that the controllable range of each stage is larger than the delay step of previous stage. As a result, the cascading DCO can provide larger delay step than DCV, the first fine-tuning stage employs 4 HDCs to reduce the number of DCV cells, leading to save power consumption. Finally, in order to further increase the DCO resolution, the 2nd and 3rd fine–tuning stages are added.

These stages employ different DCVs to improve resolution. The operation concept of DCV is to control the gate capacitance of logic gate with input state to adjust the delay time. The second and third fine-tuning stages employ 32 two–input NOR and 8 tri-state inverter, respectively. The gate capacitance of two-input NOR DCVs are changed by control signals (F2_EN [0] ~ F2_EN [31]) and the gate capacitance of tri-state inverters DCVs are changed by the control signals (F3_EN [0] ~ F3_EN [7]). As the gate capacitance of DCV changes, the delay of 2nd and 3rd fine–tuning stages can be adjusted.

**Digitally Controlled Varactors (DCVs) and Hysteresis Delay Cells (HDCs)**

Fig. 3 shows digitally controlled varactor cell (DCV) using two-input NOR gate and hysteresis delay cell (HDC). The operation concept of DCV is to control the gate capacitance of logic gate with input state to adjust the delay time. In Fig. 3, the NOR gate capacitance at node N2 depends on control node F2_EN’s value. The total gate capacitance of NOR gate varies with F2_EN input states. The equivalent circuit of two-input NOR DCV cell is shown in Fig. 3. An initial capacitance (C1) parallels with capacitance difference (∆C). The F2_EN input controls the capacitance difference (∆C) in the N2 node. A two-input NAND gate can also be applied to DCV design but it consumes more power than two-input NOR DCV so we used two-input NOR in our proposed design.

Fig. 3 also shown the HDCs used in the fine-tuning stage and each of which contains one inverter (INV2) and one tri-state inverter (TINV). As the input state of control (F1_EN [0] ~ F1_EN [3]) of TINV in HDC changes, different delay of the third fine-tuning stage can be obtained. The operation concept of HDC is to control driving current to obtain different propagation delay. When TINV of the HDC is enabled, the output signal of enable TINV has the hysteresis phenomenon in the transition state to produce different delay times from the delay chain. The propagation delay Tp from N1 to N2 is a function of loading capacitance and equivalent resistance of turn-on MOS (Rabaey, 2003) and is given by:

\[
T_p = 0.69 \frac{C_l}{R_{eq}} \left( R_{eq} + \frac{1}{2} \right)
\]

(1)

Where C_l is the loading capacitance of N2, R_{eq} and R_{eq1} are equivalent resistance of NMOS and PMOS in the driving inverter (INV1), respectively. In the general operating situation, C_l remains as constant value. But, the equivalent resistance of turn-on MOS in INV1 varies with saturation current and drain source voltage and is expressed by:

\[
R_{eq} = \frac{1}{2} \int \frac{V}{V_{DD}} \frac{V}{I_0(1 + AV)} dV
\]

(2)

where I_0 is the saturation current of transistor device. When TINV is enabled, since the input signal of TINV (N3) does not vary with the input of INV1 (N1) instantaneously, it will sink the inverse current I_3 to reduce the effective driving current from I_1 to I_2. This leads to enlarge delay time of delay chain. Fig.4 shows the hysteresis phenomenon of this HDC. In the beginning, N1 and N3 remain at high level and N2 is at low level. As N1 level changes from high to low, the signal level of N2 attempt to vary from low to high. However, because N1 remains at high level for a while (delayed by INV2), TINV sinks the inverse current to slow down.

\[\text{Fig. 3. HDC and two-input NOR DCV and its equivalent circuit with AC capacitance}\]

\[\text{Fig. 4. Hysteresis phenomenon of HDC}\]
pull-high speed of N₂. Thus, (2) should be rewritten as follow:

\[ R_{eq} = \frac{1}{VDD} \int_{VDD}^{I_DDD/2} \int_{I_D}^{I_DD} \frac{V}{I_DD - I_DD(1 + \lambda V)} dV \]  

The effective driving current changes from \( I_{1D} \) to \( I_{1D}, I_{2D} \) as \( TINV \) is enabled. In addition, based on the different driving capability tri-state inverters in a given cell library, a set of different delay steps of HDC can be constructed for specified DCO requirement.

### Performance Comparison between the Proposed Structure and Other DCO Structures

In order to performance comparison, the published approaches are designed and simulated using TSMC 180nm model and then compare with our proposed DCO. The performance comparisons are divided into three parts: coarse tuning stage comparison, path selector MUX comparison and fine tuning stage comparison.

#### Coarse-Tuning Stage Performance Comparisons

In the coarse-tuning stage, we design and simulate the conventional delay line of path-selection type by two-inverter delay cells for power consumption comparisons. For fair comparisons, both conventional and the proposed coarse-tuning stages have the same operation range. The simulation results of power consumption in different operation frequencies are shown in Table 1. As compared with conventional approaches, the proposed coarse-tuning stage can reduce 85% and 15% of power consumption at 746MHz and 225MHz, respectively. Because the number of disable redundant delay scheme has different power reduction ratio in different operation frequencies.

<table>
<thead>
<tr>
<th></th>
<th>Power@225MHz</th>
<th>Power@746MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed design</td>
<td>78.97µW</td>
<td>37.5µW</td>
</tr>
<tr>
<td>Conventional</td>
<td>90.49µW</td>
<td>243.8µW</td>
</tr>
</tbody>
</table>

### Path Selector MUX Performance Comparisons

The proposed path selector MUX architecture is implemented with transmission gates and costs less area and lower power consumption than the conventional path selector MUXs which had used tri-state buffers in their structure. In the path selector MUX stage, we design and simulate the conventional path selector MUXs by tri-state buffers for power consumption comparisons. The simulation results of power consumption are shown in Table 2. As compared with conventional approaches, the proposed path selector MUX stage can reduce 40% of power consumption at 746MHz.

<table>
<thead>
<tr>
<th></th>
<th>Power@225MHz</th>
<th>Gate Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed</td>
<td>194µW</td>
<td>48</td>
</tr>
<tr>
<td>Approach I</td>
<td>920µW</td>
<td>128</td>
</tr>
<tr>
<td>Approach II</td>
<td>410µW</td>
<td>80</td>
</tr>
</tbody>
</table>

#### Fine-Tuning Stage Performance Comparisons

In the cell-based design approach, many designs apply DCM or DCV to construct fine-tuning stage. For fair comparisons, these designs are rebuilt under the similar operation range and number of control bit. The rebuilt fine-tuning stages by different approaches are: DCV type (Approach I) (Chen et al., 2005), and combination of DCM and DCV type (Approach II) (Sheng et al., 2006). The performance comparisons simulated at 225MHz at 1.8V and typical corner cases, are summarized in Table 3.

Note that all of them have a similar performance in LSB resolution. But, in term of power consumption and area, the proposed design has significant improvement. Since the HDC can replace many DCV cells to obtain wider operating range. The number of delay cells connected with each driving inverter and loading capacitance can be reduced, leading to save power consumption and gate counts well. The reduction ratios are 79.1%, and 53.2% as compare with approach I, approach II, respectively.

### SIMULATION RESULTS

The proposed DCO is evaluated in TSMC 180nm and 1.8V power supply. The power consumption of the proposed DCO, at 205 MHz frequency is 255µW. Table 4 shows the delay step and operation range of different tuning stages in the proposed DCO. It shows that the controllable range of each stage is larger than the step of previous stage. And the finest step of 3rd fine-tuning stage determines the DCO resolution. Thus the proposed DCO can achieve high resolution with 0.95ps. In addition to DCO resolution, the proposed DCO has a good linearity as shown in Fig. 5.
Table IV: Simulation Results of Step/Range of Tuning Stage

<table>
<thead>
<tr>
<th></th>
<th>Coarse Tuning</th>
<th>1st Fine Tuning</th>
<th>2nd Fine Tuning</th>
<th>3rd Fine Tuning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range (ps)</td>
<td>3780</td>
<td>135.3</td>
<td>83.2</td>
<td>7.6</td>
</tr>
<tr>
<td>Step (ps)</td>
<td>120.12</td>
<td>38.4</td>
<td>3.18</td>
<td>0.95</td>
</tr>
</tbody>
</table>

The jitter performance of the proposed DCO is evaluated at 550MHz by monte carlo simulation using Gaussian distribution function taking into account 8% variation in supply voltage. Simulation results are shown in Fig. 6, by overlapping every cycle period. A 90ps time-period Jitter is measured.

![Fig. 5. Linearity of DCO](image)

![Fig. 6. Time-period jitter of the proposed DCO (Monte Carlo analysis)](image)

Table 5 lists the comparisons with a few recent state-of-the-arts DCO designs. The proposed DCO achieves the finest LSB resolution and the highest operating frequency. In addition, the proposed DCO consumes less power than the others.

![Table 5](image)

**CONCLUSION**

In this paper, an ultra low power and high-resolution DCO has been proposed. Proposed DCO has a segmental course-tuning stage and a fine-tuning stage with three substages which are implemented with HDC and different DCVs. also it has a proposed multistage path selector MUX which apply transmission gates in its structure and costs less area and lower power consumption than the conventional path selector MUXs which had used tri-state buffers in their structure. Simulation of the proposed DCO using TSMC 180nm model achieves a frequency of 205MHz – 925MHz and power consumption of 255µW at 205 MHz and 1.8V power supply and 0.95ps resolution.

**REFERENCES**


